

Fig. 2

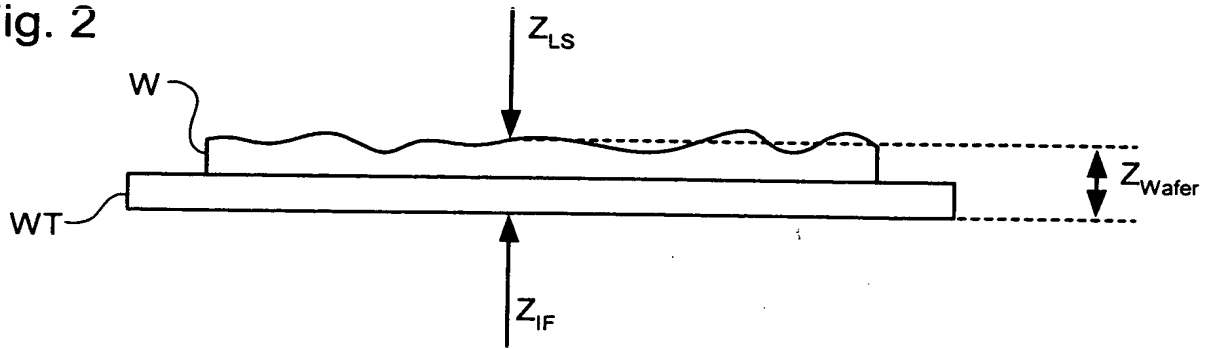


Fig. 3

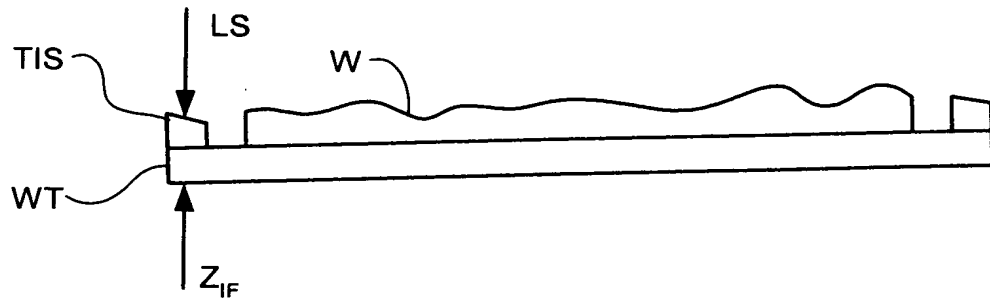


Fig. 4

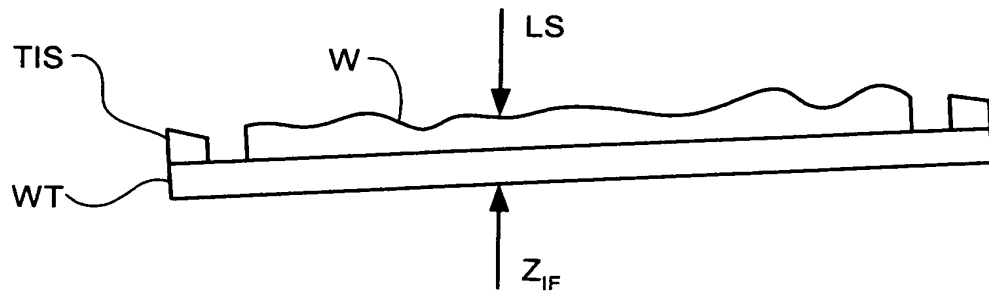


Fig. 5

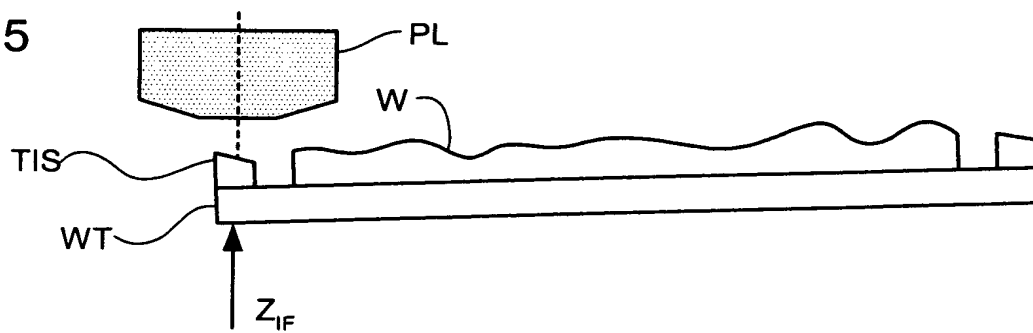


Fig. 6

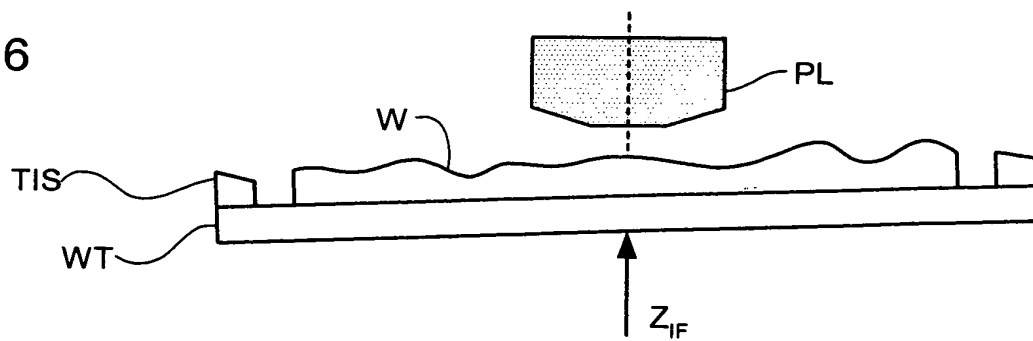


Fig. 7

TIS2

F

WT

W

F

TIS1

```

graph TD
    WI[WAFER IN] --> S1((LOAD))
    S1 -- S1 --> S2((INIT PSD))
    S2 -- S2 --> S3((LS+AA1))
    S3 -- S3 --> S4((LS+AA2))
    S4 -- S4 --> S5((GLC))
    S5 -- S5 --> S6((W1 + W2))
    S6 -- S6 --> S7((PDC))
    S7 -- S7 --> S8((VACUUM))
    S8 -- S8 --> S9((Z-MAP))
    S9 -- S9 --> S10((AA))
    S10 -- S10 --> S11((SWAP))
    S11 -- S11 --> S12((UNLOAD))
    S12 -- S12 --> WO[WAFER OUT]
    S12 -- S12 --> S1
  
```

The flowchart illustrates the process flow between TIS 1 and TIS 2. It includes the following steps and transitions:

- INIT PSD** (Step S14) leads to **TIS 1** (Step S16).
- LOAD MA** (Step S15) leads to **TIS 1** (Step S16).
- TIS 1** (Step S16) leads to **TIS 2** (Step S17).
- TIS 2** (Step S17) leads to **MA EXCH** (Step S20).
- MA EXCH** (Step S20) leads to **EXPOSE** (Step S18).
- EXPOSE** (Step S18) leads to **SWAP** (Step S13).
- SWAP** (Step S13) leads to **INIT PSD** (Step S14).
- EXPOSE** (Step S18) leads to **SYS CAL** (Step S19).
- SYS CAL** (Step S19) leads to **EXPOSE** (Step S18).
- TIS 2** (Step S17) also leads directly to **SYS CAL** (Step S19).

Steps **TIS 1**, **TIS 2**, **EXPOSE**, and **SWAP** are represented by hatched ovals, while **INIT PSD**, **LOAD MA**, **MA EXCH**, and **SYS CAL** are represented by plain ovals.

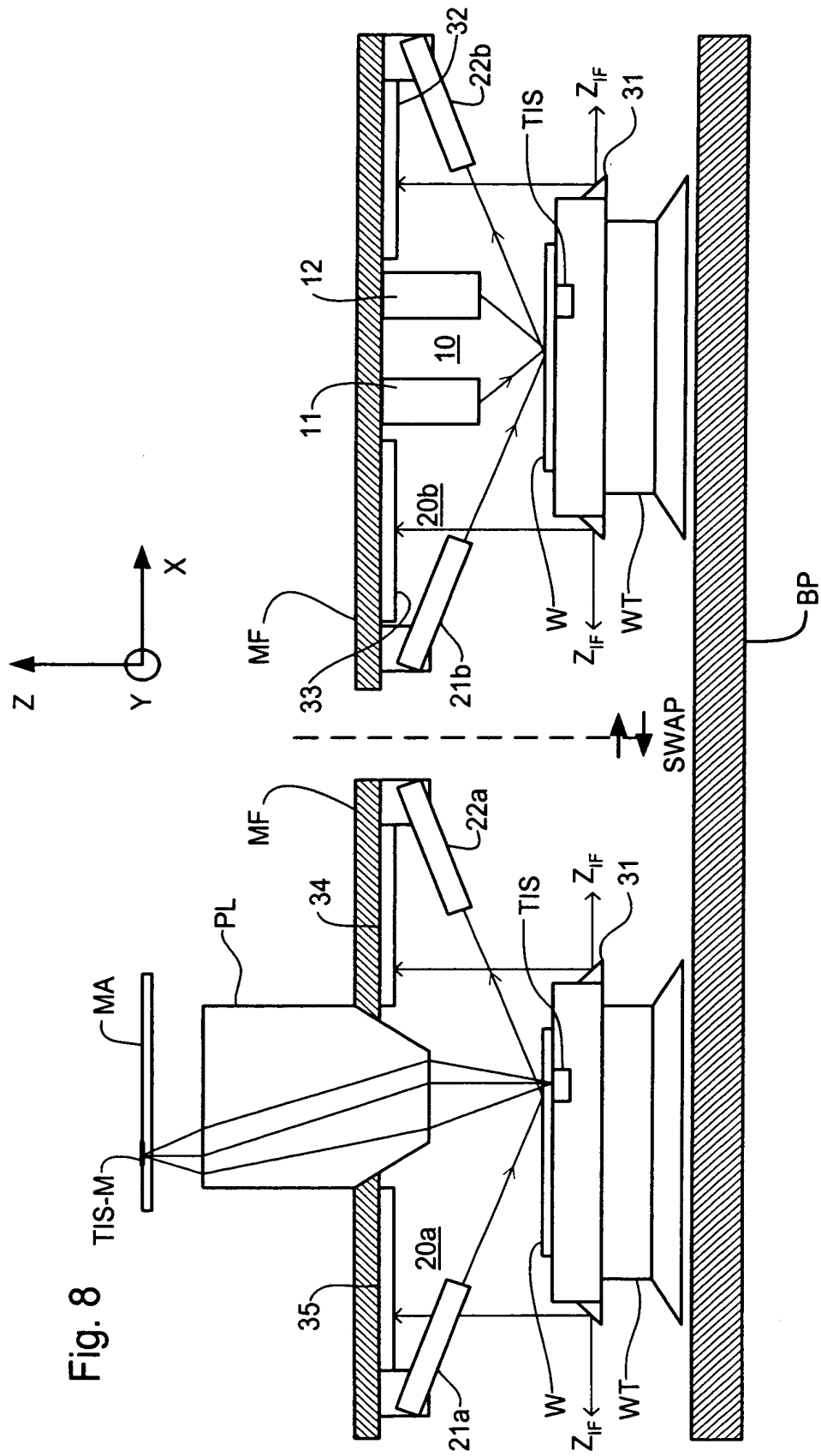


Fig. 11

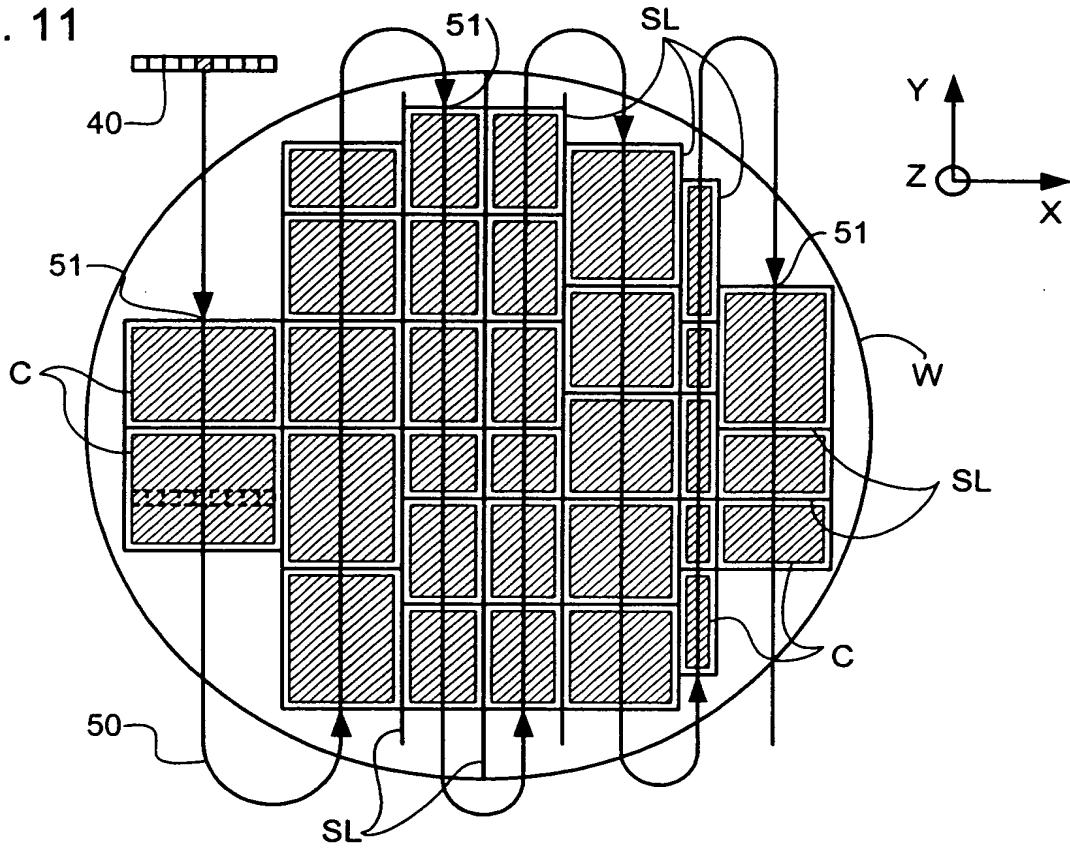


Fig. 12

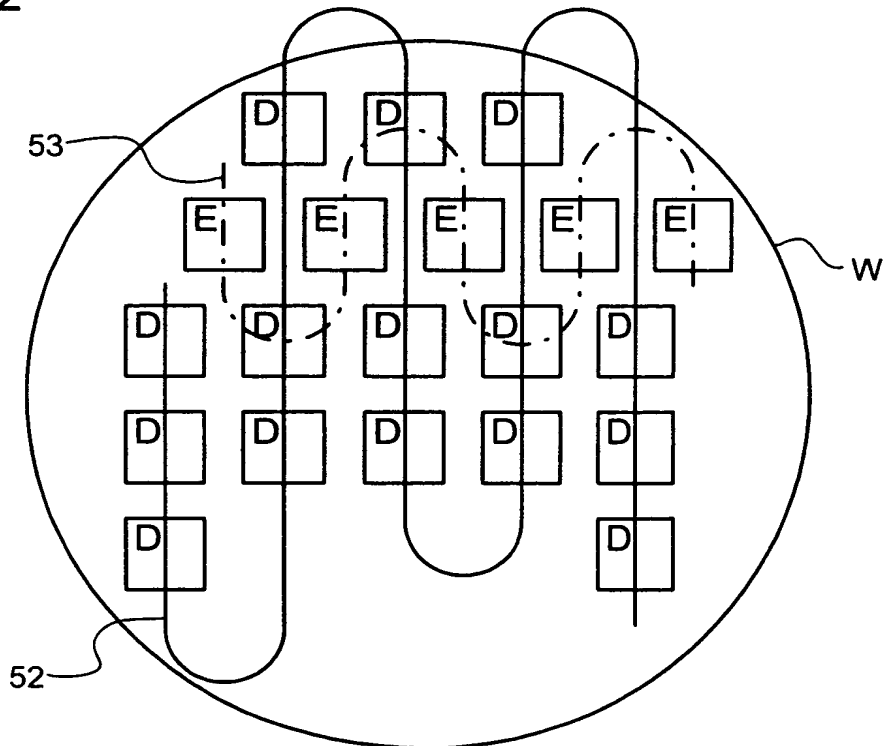


Fig. 13

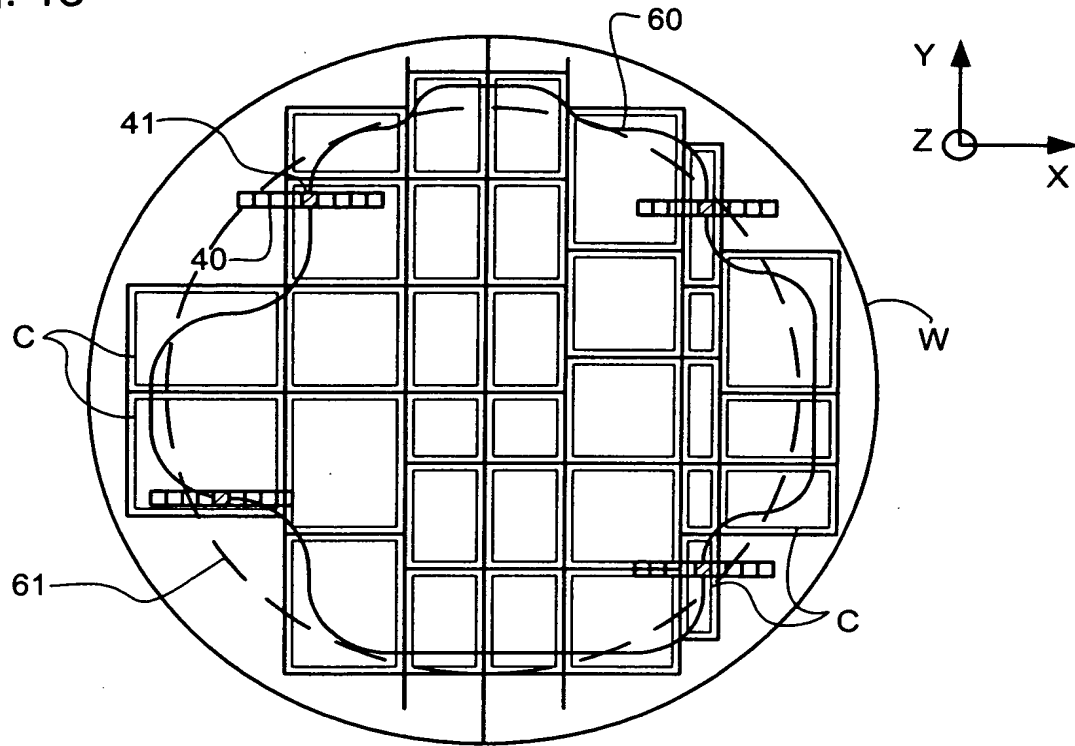


Fig. 15

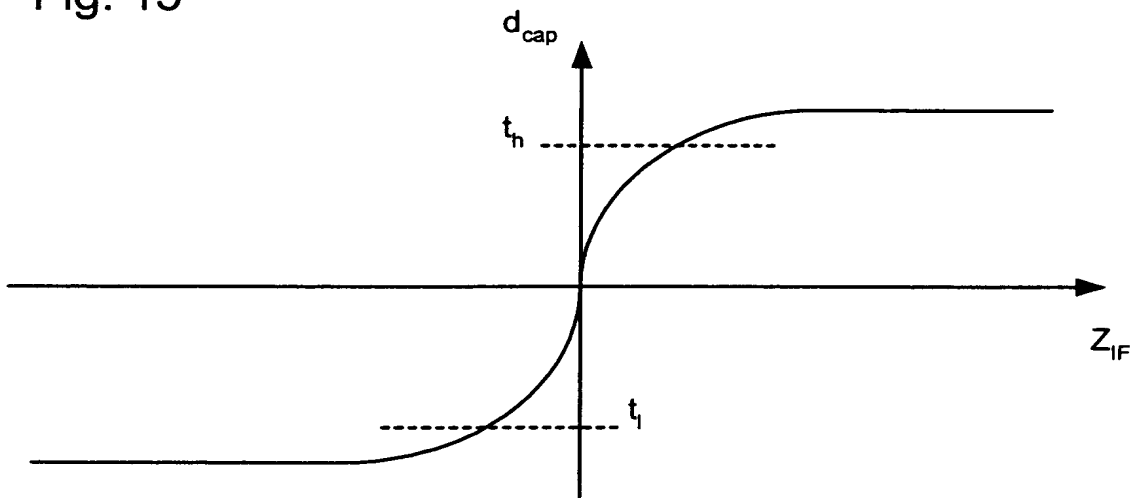
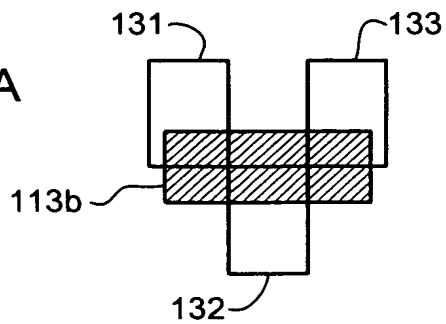


Fig. 15A



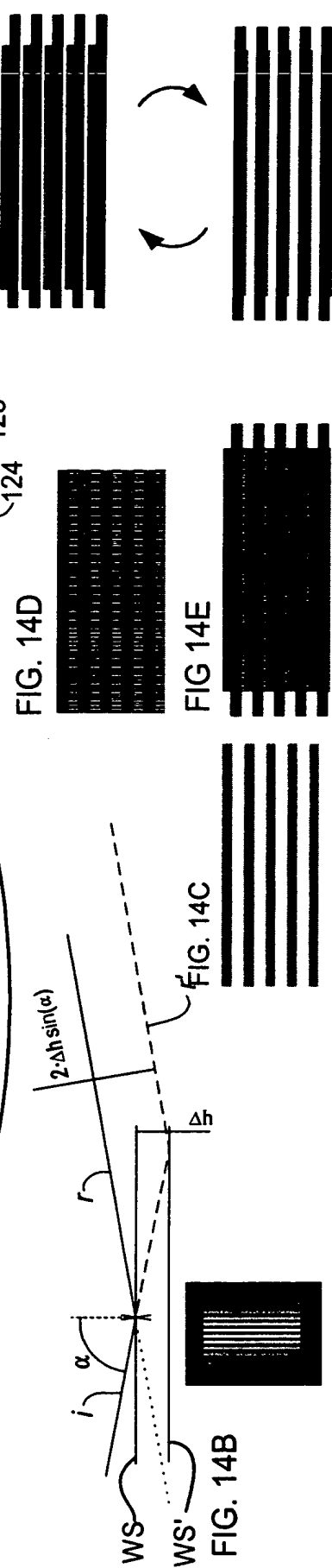
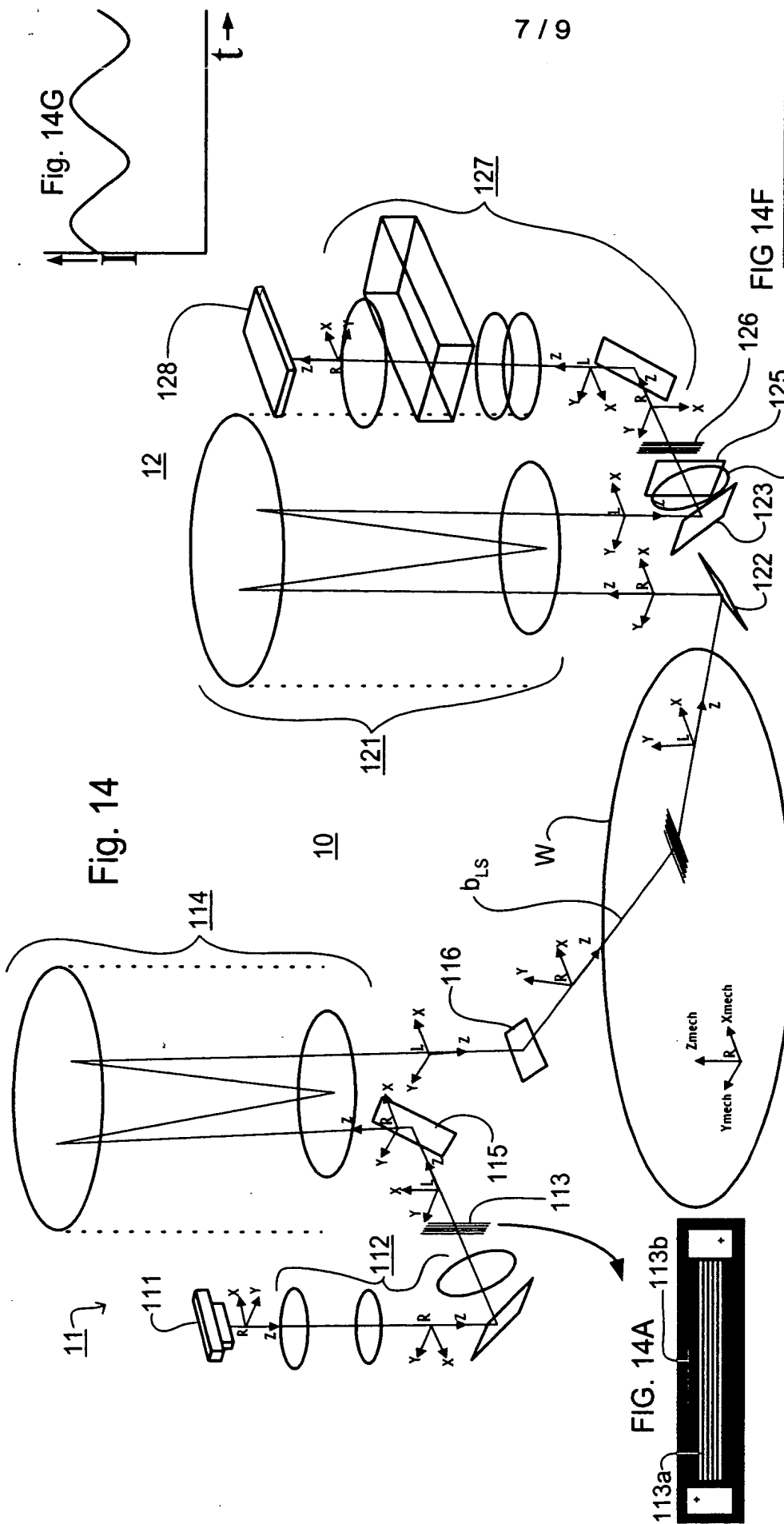


Fig. 16

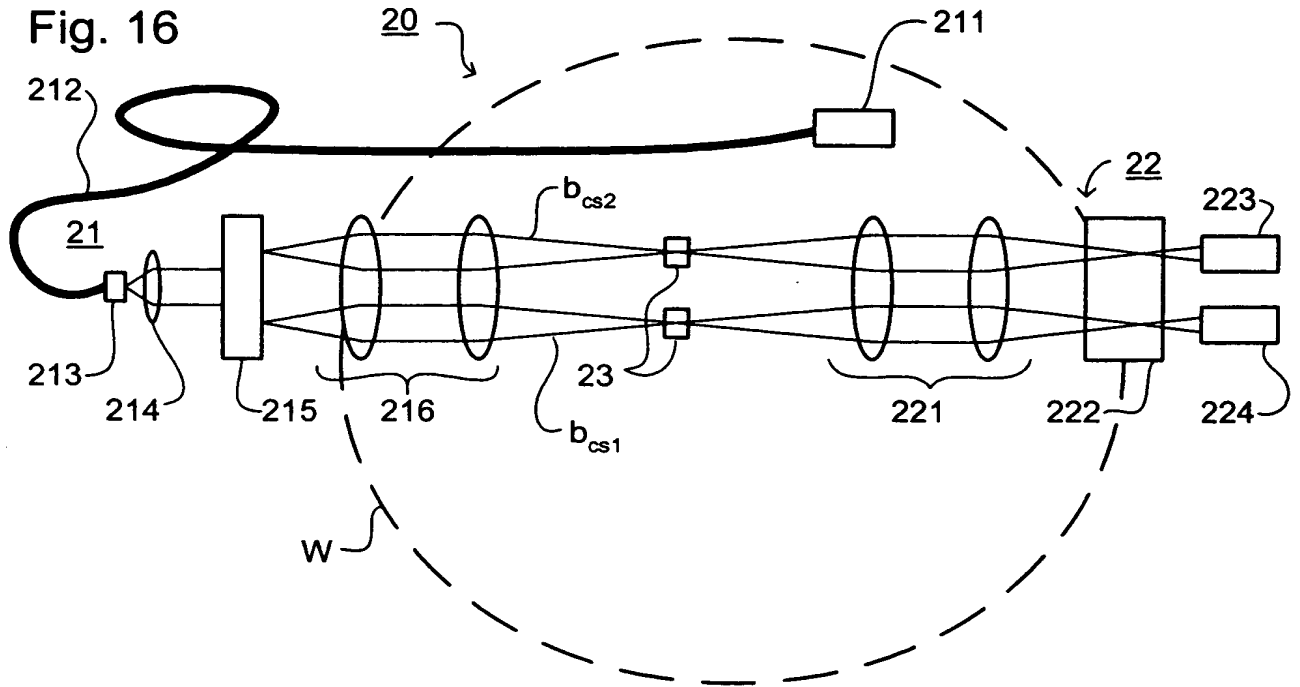


Fig. 17

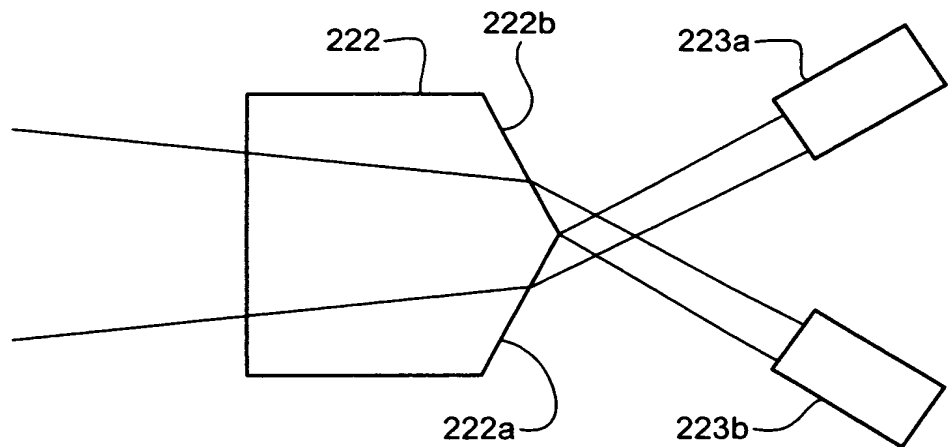


Fig. 18

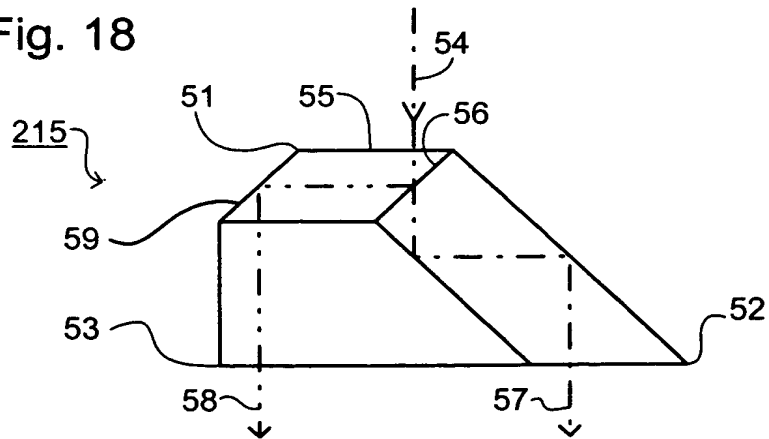


Fig. 19

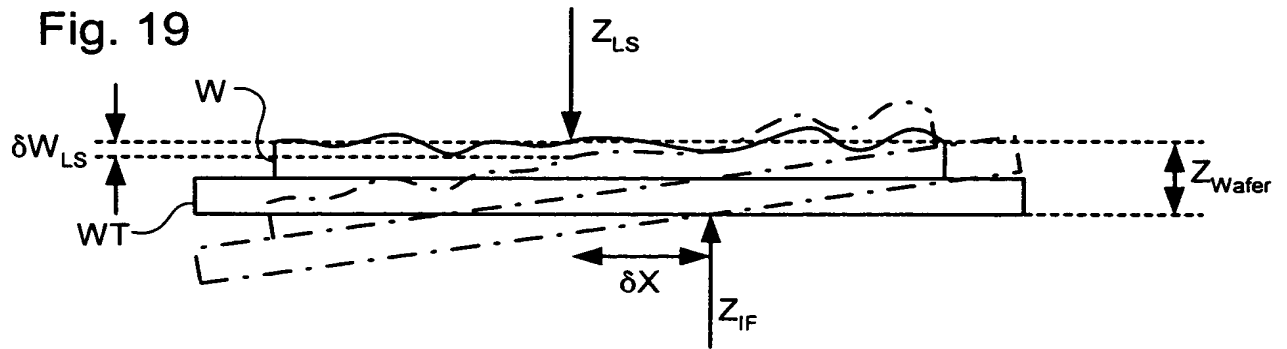


Fig. 20

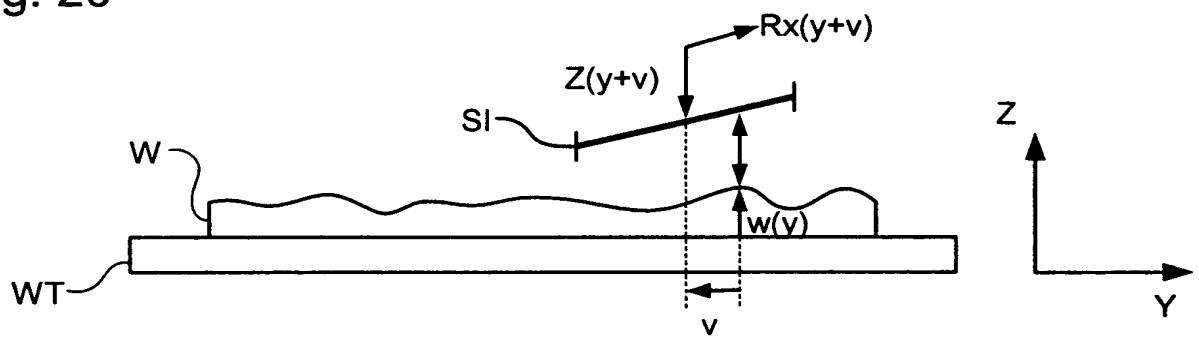


Fig. 21

